WiP: FPGA implementation of Synchronous Serial Interface for Hardware in Loop Simulation

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WiP: FPGA implementation of Synchronous Serial Interface for Hardware in Loop Simulation

Objective: SSI protocol implementation in FPGA layer of a Real time Simulator

Need: Limitation of DO, Encoder hardware elimination

Basic Synchronous Serial Interface Communication

HiL Setup
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Implementation:

\[
\text{timeout counter} = \frac{\text{INT board clock period} - (\text{Max resolution} \times \text{pulse period})}{\text{FPGA clock period}}
\]

<table>
<thead>
<tr>
<th>Clock Rising Edge</th>
<th>Clock Falling Edge</th>
<th>Counter Value</th>
<th>Transmitted Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0/1</td>
<td>0</td>
<td>0</td>
<td>Load Parallel Data</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Set to 2000</td>
<td>Send the last transmitted bit</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0&lt;Counter Value&lt;2000</td>
<td>Send the next bit</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0&lt;Counter Value&lt;2000</td>
<td>Send the last transmitted bit</td>
</tr>
</tbody>
</table>

Redundancy: Two separate Clock pulse is received and two separate serial data are sent out
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Results:

Motor Speed = 30rpm

SSI Redundancy