WiP: FPGA implementation of Synchronous Serial Interface for Hardware in Loop Simulation

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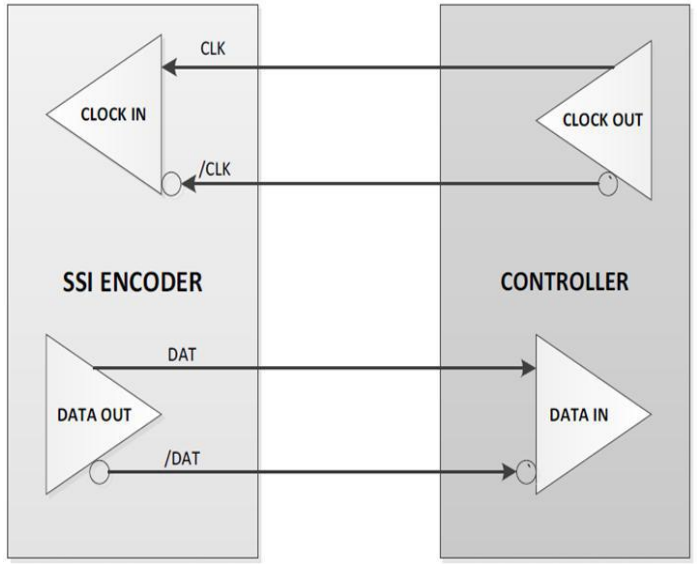
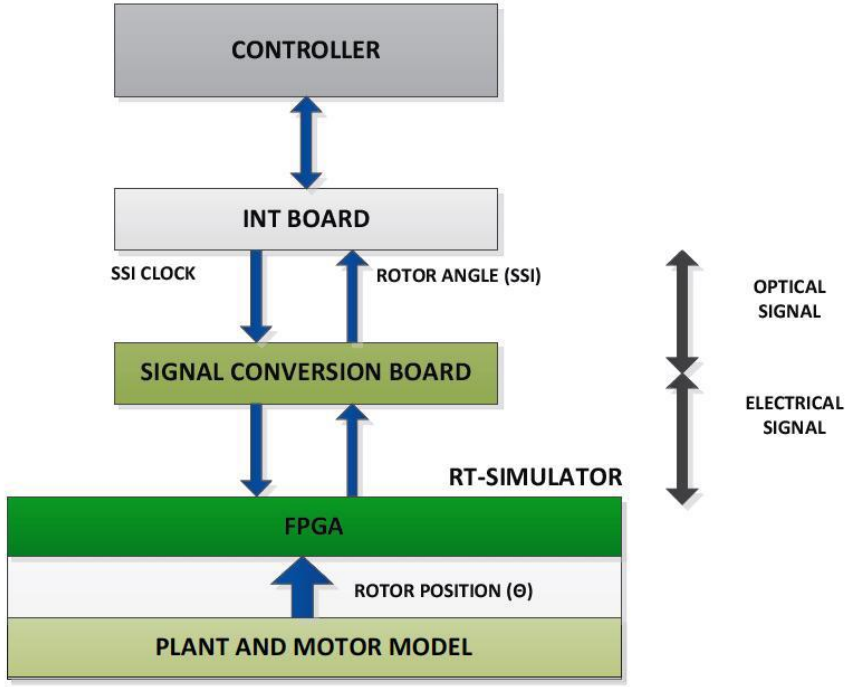
Objective: SSI protocol implementation in FPGA layer of a Real time Simulator

Need: Limitation of DO, Encoder hardware elimination



Basic Synchronous Serial Interface Communication



HiL Setup

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Implementation:

$$timeout\ counter = \frac{INT\ board\ clock\ period - (Max\ resolution * pulse\ period)}{FPGA\ clock\ period}$$

Clock Rising Edge	Clock Falling Edge	Counter value	Transmitted Data
0/1	0	0	Load Parallel Data
0	1	Set to 2000	Send the last transmitted bit
1	0	0<Counter Value<2000	Send the next bit
0	0	0<Counter Value<2000	Send the last transmitted bit

Redundancy: Two separate Clock pulse is received and two separate serial data are sent out

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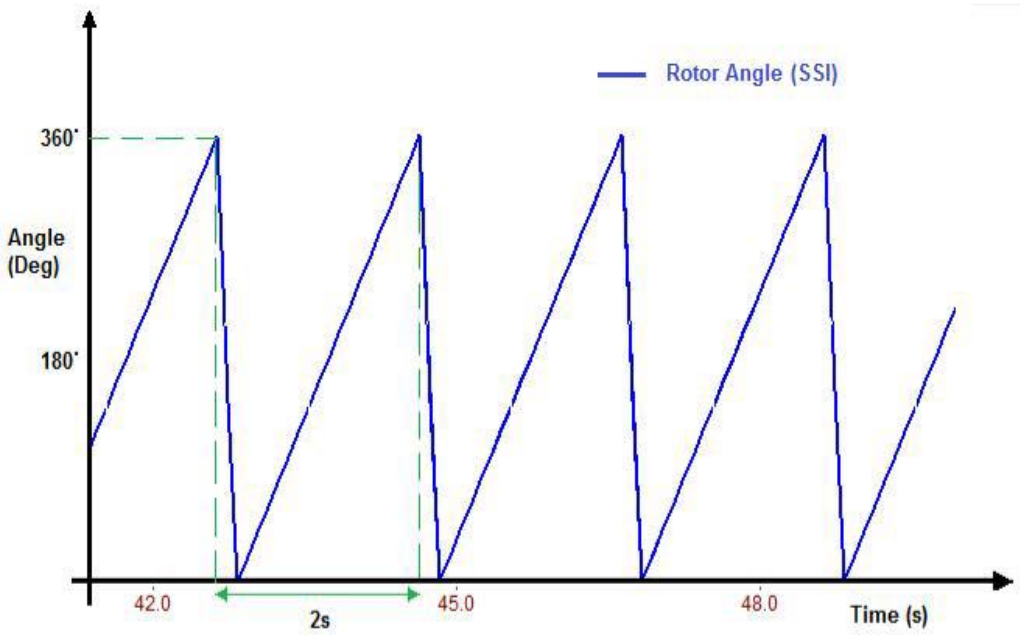
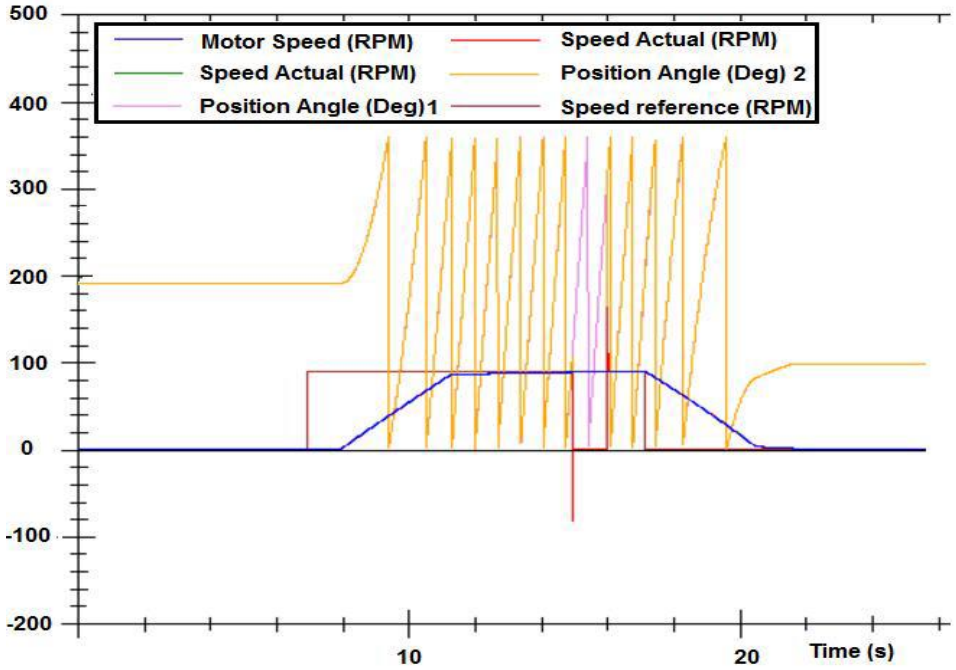
Results:



Motor Speed = 30rpm



SSI Redundancy